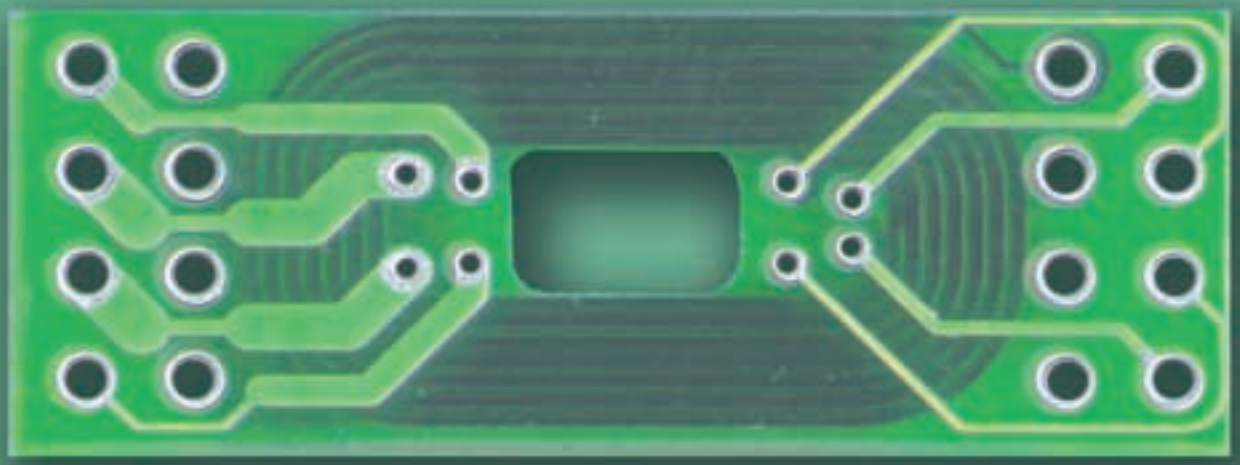
Application Note

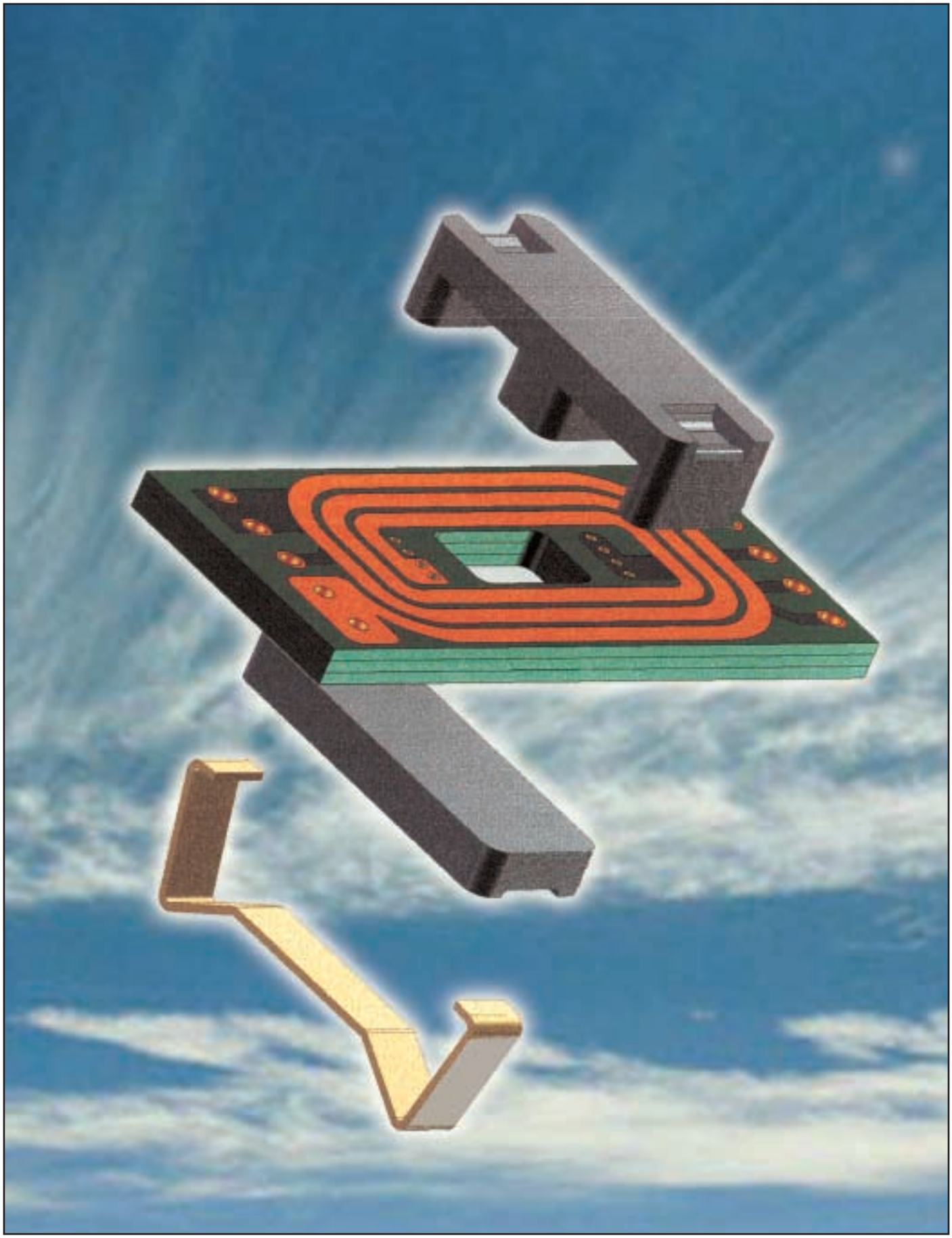
Design of Planar Power Transformers



FERROXCUBE
A YAGEO COMPANY

Design of Planar Power Transformers

Contents



Exploded view of a planar transformer

Introduction

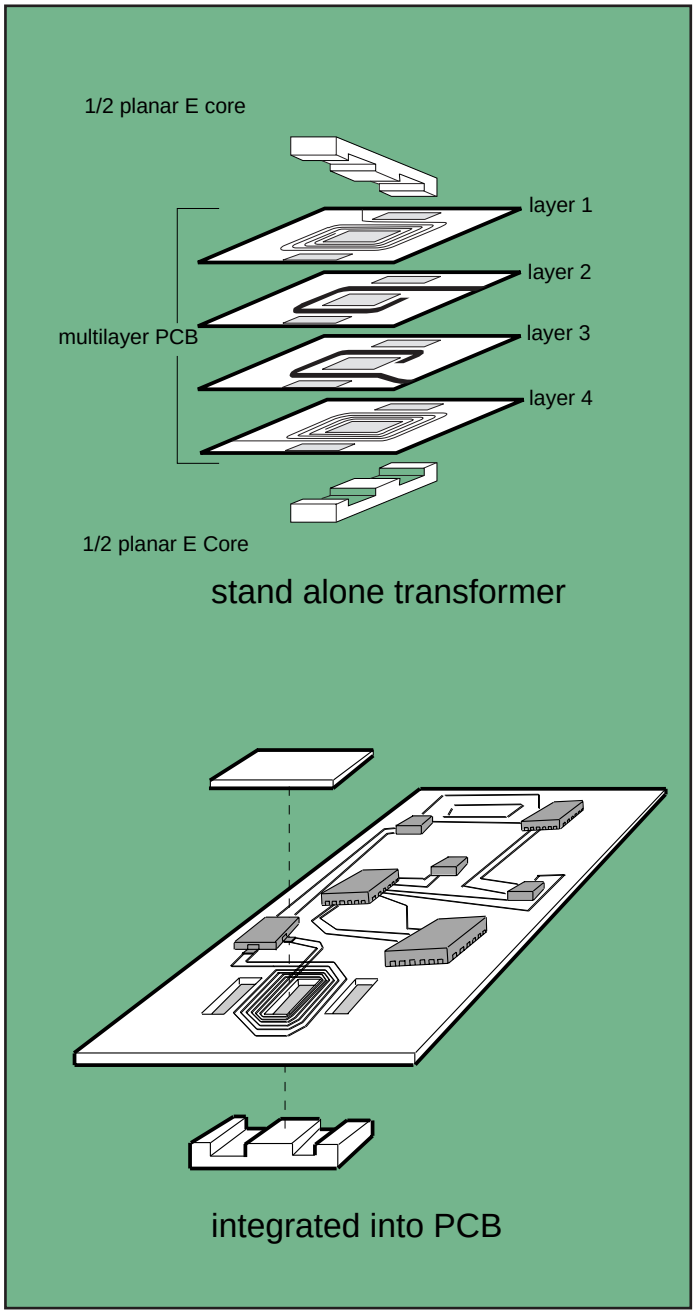
Planar transformers can be constructed as stand alone components, with a stacked layer design or a small multilayer PCB, or integrated into a multilayer board of the power supply.

Important advantages of planar magnetics are:

- very low profile
- excellent thermal characteristics.
- low leakage inductance
- excellent repeat ability of properties

Measurements on planar E core transformers under operating conditions with windings in multilayer PCBs show that the thermal resistance is substantially lower (up to 50 %) compared to conventional wire wound transformers with the same effective core volume V_e. This is caused by the improved surface to volume ratio. The result of this better cooling capability is that planar transformers can handle higher throughput power densities, while the temperature rise is still within acceptable limits.

This brochure presents a fast and easy method to make designs for planar power transformers.
Examples which have been designed with this fast procedure will be discussed.
Tests under operating conditions show that the measured results are in good agreement with the predicted temperature rise.



Planar principles

Design procedure

1. Calculation of maximum flux density

The core and copper losses in a transformer under operating conditions will induce a temperature rise. This rise must stay below a maximum allowable value to avoid damage to the transformer or the rest of the circuitry. In thermal equilibrium the total losses in the transformer, P_{trafo}, can be related to a temperature rise ΔT of the transformer with an analogon of Ohm's law by:

$$P_{trafo} = \frac{\Delta T}{R_{th}} \qquad [1]$$

In this formula R_{th} represents the thermal resistance of the transformer. P_{trafo} can in fact be interpreted as the cooling capability of the transformer.
Previous work [1], showed that it is possible to establish an empirical formula which relates the value of thermal resistance of a transformer directly to the value of the effective magnetic volume V_e of the ferrite core used. This empirical formula is valid for wire wound transformers with core shapes like RM and ETD. A similar relation has now been found for planar E transformers.
This relation can be used to estimate the temperature rise of the transformer as a function of flux density in the core. Because of the limited available winding space it is recommended to use the maximum allowed flux densities in planar magnetics.
With the assumption that half of the total transformer loss is core loss, it is possible to express the maximum core loss density P_{core} as a function of the allowed temperature rise ΔT of the transformer as:

$$P_{core} = \frac{12 \cdot \Delta T}{\sqrt{V_e\ (cm^3)}} \quad [mW/cm^3] \qquad [2]$$

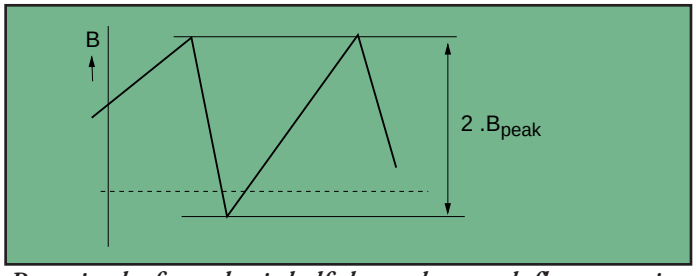
Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated [2] by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \qquad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{peak}^y \quad [mW/cm^3]$$

In this formula C_m, x ,y, ct_0, ct_1 and ct_2 are parameters which have been found by curve fitting of the measured power loss data. These parameters are specific for a ferrite material. They are dimensioned in such a way that at 100 °C the value of C_T is equal to 1.
In table 1 fit parameters are listed for several Ferroxcube power ferrites. Maximum allowed P_{core} is calculated with equation [2]. This value is inserted in equation [3]. Maximum allowed flux density B_{peak} can now be calculated by rewriting equation [3]:

$$B_{peak} = \left[\frac{P_{core}}{C_m \cdot C_T \cdot f^x} \right]^{1/y} \quad [T] \qquad [4]$$



B_{peak} in the formulas is half the peak to peak flux excursion in the core.

ferrite	f (kHz)	Cm	x	y	ct_2	ct_1	ct_0
3C30	20-100	$7.13.10^{-3}$	1.42	3.02	$3.65.10^{-4}$	$6.65.10^{-2}$	4
	100-200	$7.13.10^{-3}$	1.42	3.02	4.10^{-4}	$6.8 .10^{-2}$	3.8
3C90	20-200	$3.2.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3C94	20-200	$2.37.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
	200-400	2.10^{-9}	2.6	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3F3	100-300	$0.25.10^{-3}$	1.63	2.45	$0.79.10^{-4}$	$1.05.10^{-2}$	1.26
	300-500	2.10^{-5}	1.8	2.5	$0.77.10^{-4}$	$1.05.10^{-2}$	1.28
	500-1000	$3.6.10^{-9}$	2.4	2.25	$0.67.10^{-4}$	$0.81.10^{-2}$	1.14
3F4	500-1000	12.10^{-4}	1.75	2.9	$0.95.10^{-4}$	$1.1.10^{-2}$	1.15
	1000-3000	$1.1.10^{-11}$	2.8	2.4	$0.34.10^{-4}$	$0.01.10^{-2}$	0.67

Table 1: Fit parameters to calculate the power loss density

Note:
The maximum allowed value for B can also be found in another way. Formula [3] together with the fit parameters can be inserted into a computer program which makes it possible to calculate the power losses for arbitrary wave forms (3). Advantage is that the real wave shape of B can be simulated to calculate the losses and that it is possible to select the optimum ferrite for the concerned application.

2. Recommendations for distribution of the turns in the winding space

Once the value for the maximum peak flux density is determined, established formulas applicable to the converter topology and transformer type (e.g. flyback or forward) can be used to calculate the number of primary and secondary turns.

A decision has to be made how the windings will be divided over the available layers. Currents in the tracks will induce a temperature rise of the PCB. It is recommended to distribute the winding turns in the outer layers symmetrically with respect to the turns in the inner layers for reasons of thermal expansion.
From a magnetic point of view the optimum would be to sandwich the primary and secondary layers. This will reduce the so called proximity effect (see page 6).
However the available winding height in the PCBs and the required number of turns for the application will not always allow an optimum design.

For cost price reasons it is recommended to choose a standard thickness of the copper layers. Often a thickness of 35 or 70 µm are used by PCB manufacturers. The choice of thickness of the layers plays an important role for the temperature rise in the windings induced by the currents.

Safety Standards like IEC 950 require a distance of 400 µm through PCB material (FR2 or FR4) for mains insulation between primary and secondary windings. If mains insulation is not required a distance of 200 µm between the winding layers is sufficient. Furthermore one has to take into account a solder mask layer of about 50 µm on the top and bottom of the PCB.

The track width of a winding follows from the value of the current and the maximum current density allowed. The spacing between the turns is governed by the production capabilities and costs. A rule of thumb for a copper layer thickness of 35 µm is a track width and spacing of > 150 µm, and for layers of 70 µm >200 µm.

Depending on the production capability of the PCB manufacturer smaller dimensions might be possible, but that will probably imply a substantial cost increase of the PCB.
The number of turns per layer and the spacing between the turns are denoted by the symbols N_l and s respectively. Then for an available winding width b_w , the track width w_t can be calculated with (see fig 1):

$$w_t = \frac{[\, b_w - (N_l + 1) \,.\, s \,]}{N_l} \qquad [5]$$

In case mains insulation requirements have to be fulfilled the situation is somewhat different. The core is seen as a part of the primary side and has to be separated 400 µm from the secondary side. Therefore, the creepage distance between the (secondary) windings close to the inner and outer leg and the core must be 400 µm. In this case the track width can be calculated with [6] since 800 µm has to be subtracted from the available winding width.

$$w_t = \frac{[\, b_w - 0.8 - (N_l - 1) \,.\, s \,]}{N_l} \qquad [6]$$

In formula 5 and 6 all dimensions are in mm.

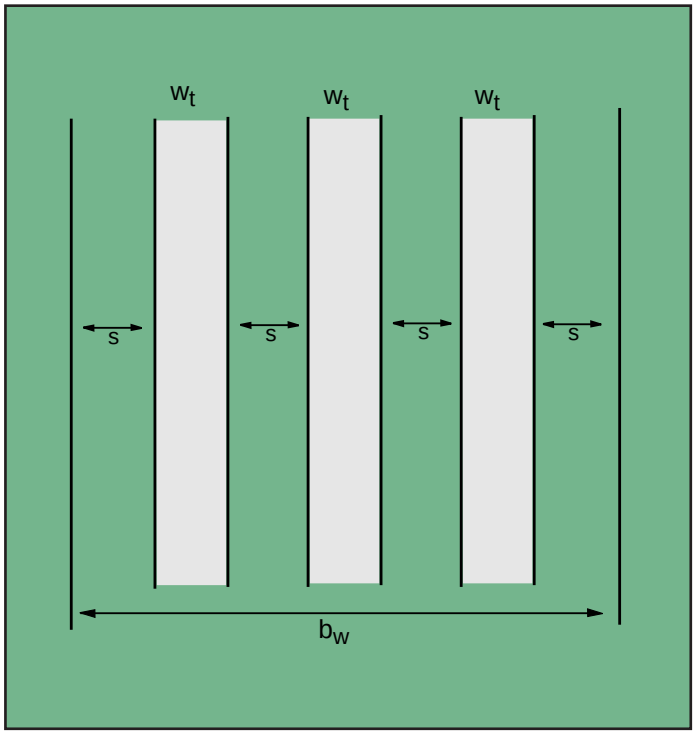


Fig.1 Track width w_t spacing s and winding width b_w

3. Determination of temperature rise in the PCB caused by the currents

The final step is to check the temperature rise in the copper tracks induced by the currents. For this purpose the effective (= RMS) currents have to be calculated from the input data and desired output. The calculation method depends on the topology used. In the design examples this is shown for a conventional standard forward and flyback converter topology. An example of relations between the RMS currents and induced temperature rises for various cross sections of conductors in PCBs is shown in fig. 2. For single conductor applications or inductors which are not too closely spaced this chart can be used directly for determining conductor widths, conductor thickness, cross sectional areas and allowed maximum currents for various preset values of the temperature rise.

Note:
For groups of similar parallel inductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and equivalent current. The equivalent cross section is the sum of the cross sections of the parallel conductors and the equivalent current is the sum of the currents in the inductor.

A shortcoming in this design approach is that the induced heat in the windings is assumed to be caused by a DC current while in reality there is an AC current causing skin effect and proximity effect.
The skin effect is the result of the magnetic field inside a conductor generated by the conductors own current. Fast current changes (high frequency) induce alternating fluxes which cause eddy currents. These eddy currents which add to the main current are opposite to the direction of the main current. The current is cancelled out in the centre of the conductor and moves towards the surface. The current density decreases exponentially from the surface towards the centre.

The skin depth δ is the distance from the conductor surface towards the centre over which the current density has reduced by a factor of 1/e. The skin depth depends on material properties as conductivity and permeability and is inversely proportional to the square root of the frequency. For copper at 60 °C the skin depth can be approximated by: $\delta(\mu m) = 2230/(f\ [kHz])^{1/2}$.
When the conductor width (w_t) is taken smaller than 2δ, the contribution of this effect will be limited.This means a track width of <200 µm for a frequency of 500 kHz.
If there is more winding width b_w available for the concerned number of turns, the best solution from the magnetic point of view would be to split them up in parallel tracks.

In practical situations there will be eddy current effects in the conductor not only due to the alternating field of its own current (skin effect) but also due to the fields of other conductors in the vicinity. This effect is called the proximity effect. When the primary and secondary layers are sandwiched this effect will be strongly decreased. Reason is that the primary and secondary currents flow in opposite directions so that their magnetic fields will cancel out. However there will still be a contribution to the proximity effect of the neighbouring conductors in the same layer.

Empirical tool
Temperature measurements on several designs of multilayer PCBs with AC currents supplied to the windings, show with reasonable accuracy that up to 1MHz each increase of 100 kHz in frequency gives 2 °C extra in temperature rise of the PCB compared to the values determined for DC currents.

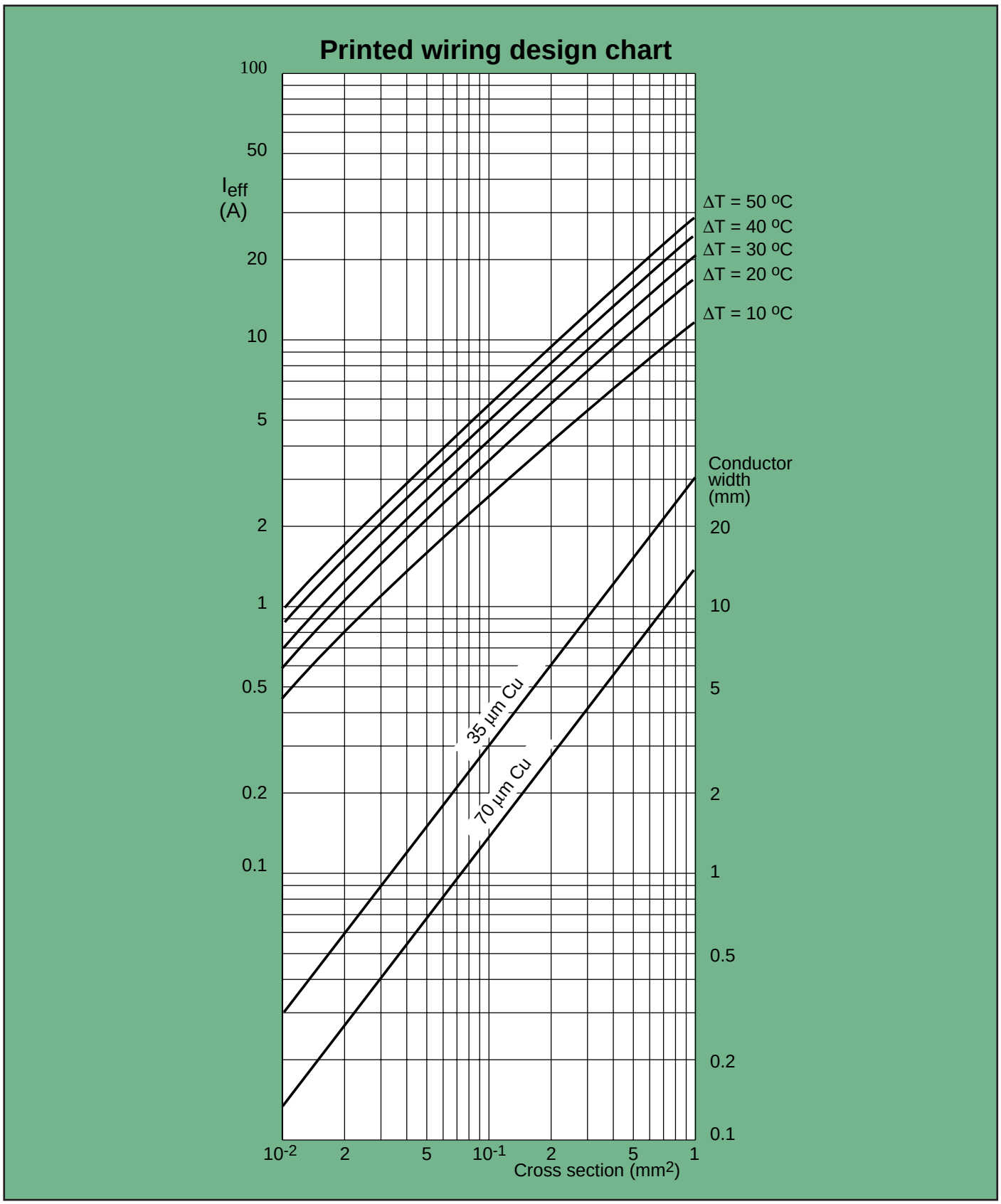


Fig.2 Relation between current, dimensions of tracks in PCBs and temperature rise.

Design example 1: Flyback transformer

minimum input voltage:	Uimin	= 70 V
output voltage:	Uo	= 8.2 V
extra primary output:	Up_{IC}	= 8V
primary duty cycle:	δ_{prim}	≈ 0.48/0.5
secondary duty cycle:	δ_{sec}	≈ 0.48/0.5
switching frequency	f	≈120kHz
output power	P_{max}	8 W
ambient temperature	T_{amb}	60ºC
allowed temperature rise	ΔT	35ºC

The aim is to design a flyback transformer with a specification as shown above.
As a first step it is assumed that at this frequency a high peak flux density of 160 mT can be used. Later it will be checked whether this is possible given the allowed core losses and temperature rise.
Table 2 shows the calculated number of turns for the six smallest standard combinations of the Ferroxcube planar E and PLT cores. Also the primary self inductance and required airgaps and currents are calculated with formulas as shown in appendix 1.

From Table 2 it can be seen that he required number of primary turns for the E-14 core sets is too high for a multilayer PCB winding. Therefore an E-E18 or E-PLT18 core combinations look the most suitable choice. Rounding of N_1, N_2 and N_{IC} results in 24, 3 and 3 respectively.

A program based on expression [3] is used to compute the losses for unipolar triangle flux wave forms with frequency 120 kHz, B_{peak} 160 mT and operating temperature 95 °C. For the power ferrites 3C30, 3C90 the expected core loss densities are 385 mW/cm^3 and 430 mW/cm^3.

Allowed core loss densities for ΔT = 35 °C are 470 mW/cm^3 for E-PLT18 and 429 mW/cm^3 for E-E18 (from equation 1).
The conclusion is that 3C30 and 3C90 can be used in both core combinations. Inferior ferrites with higher power losses would result in a too high temperature rise.

The 24 primary winding turns can be divided in a symmetrical way by using 2 or 4 layers. The available winding width of the E-18 cores is 4.6 mm. This implies it will be a technically difficult - and therefore expensive - solution to use only 2 layers with 12 turns each. This would require very narrow track widths and spacing.
So a choice is made for 4 layers with 6 turns each.
A lower number of layers in the multilayer PCB will result in a lower cost price. Therefore we assume for the 3 turns of the primary (for IC voltage) and for the 3 secondary winding turns one layer each. The six layer design could be built up as shown in table 3.

Core	A_e (mm^2)	V_e (mm^3)	N_1	N_2	N_{IC}	G(μm)	Other calculated data
E-PLT14	14.5	240	63	7.4	7.2	113	Lprim = 638 μH
E-E14	14.5	300	63	7.4	7.2	113	Ip(RMS)=186 mA
E-PLT18	39.5	800	23	2.7	2.6	41	Io(RMS)= 1593 mA
E-E18	39.5	960	23	2.7	2.6	41	
E-PLT22	78.5	2040	12	1.4	1.4	22	
E-E22	78.5	2550	12	1.4	1.4	22	

Table 2. Calculation of data for several flyback transformers.

Depending on the heat generated by the currents the choice can be made between 35 or 70 µm copper layers. Between primary and secondary layers a distance of 400 µm is required for the mains insulation. An E-PLT 18 combination has a minimum winding window of 1.8.mm. This is sufficient for the 35 µm layer design which results in a PCB thickness of about 1710 µm.
To achieve a economic design we assumed a spacing of 300 µm between the tracks. Calculating the track width for the secondary winding with [5] returns 1.06 mm, inclusive mains insulation.
Looking in fig 2. and using the calculated (see table 2) secondary RMS current of 1.6 A, results in a temperature rise of 25 °C for the 35 µm layers and approx. 7 °C for the 70 µm design.
The temperature rise caused by the winding loss is allowed to be about half the total temperature rise, in this case 17.5 °C. Clearly the 35 µm layers will give a too large temperature rise for an RMS current of 1.6 A and the 70 µm layers will have to be used.
The track widths for the primary winding turns can be calculated with [5] and will be approx. 416 µm. This track width will cause hardly any temperature rise by the primary RMS current of 0.24 A.
Because the frequency is 120 kHz, 2 °C extra temperature rise of the PCB is expected compared to the DC current situation. The total temperature rise of the PCB caused by the currents only will remain below 10 °C.

This design with 6 layers of 70 µm Cu tracks should function within its specification. The nominal thickness of the PCB will be about 1920 µm which means that a standard planar E-PLT18 combination cannot be used. The standard E-E18 combination with a winding window of 3.6 mm is usable. However its winding window is excessive, so a customized core shape with a winding window of approximately 2 mm would be a more elegant solution.

Measurements on a comparable design with an E-E core combination in 3C90 material showed a total temperature rise of 28 °C. This is in line with a calculated contribution of 17.5 °C temperature rise from the core losses and 10 °C caused by winding losses.
The coupling between primary and secondary is good because the leakage inductance turns out to be only 0.6 % of the primary inductance.

Layers	Turns	35 µm	70 µm
solder mask		50 µm	50 µm
primary	6	35 µm	70 µm
insulation		200 µm	200 µm
primary	6	35 µm	70 µm
insulation		200 µm	200 µm
primary IC	3	35 µm	70 µm
insulation		400 µm	400 µm
secondary	3	35 µm	70 µm
insulation		400 µm	400 µm
primary	6	35 µm	70 µm
insulation		200 µm	200 µm
primary	6	35 µm	70 µm
solder mask		50 µm	50 µm
TOTAL		1710 µm	1920 µm

Table 3. Example of a six layers design

Design example 2: Forward transformer

input and output voltages:	48 V	5 V
	48 V	3.3 V
	24 V	5 V
	24 V	3.3 V
output power:	Pmax	≈ 18 W
duty cycle:	δ	≈ 0.46
switching frequency	f	≈ 500kHz
ambient temperature	T_{amb}	= 40°C
allowed temperature rise	ΔT	= 50°C

Here the aim is to design a forward transformer with the possibility to choose from 4 transformation ratios which are often used in low power DC-DC converters. The specification is shown above.
The first step is to check whether the smallest core combinations of the standard planar E core range, the E-PLT14 and E-E14, are suitable for this application. Using [2] to calculate the allowed core loss density for a temperature rise of 50 °C results in 1095 mW/cm^3 and 1225 mW/cm^3 for the E-E and E-PLT 14 combinations . With formula [3] the core loss density is calculated for unipolar triangle flux wave forms with a frequency of 500 kHz and several peak flux densities. It turns out that peak flux densities of about 100 mT will result in losses lower than the allowed core loss densities calculated with [2].

The calculation of the winding turns and effective currents is done with the formulas given in appendix 1. Using a peak flux density of 100 mT, together with the specified data as input for the calculation, it turns out that at a frequency of 530 kHz the E-E14 or the E-PLT14 are usable core combinations with a reasonable number of turns .The results of the calculations are shown in table 4.

A final check of the core loss density at the operating temperature of 100 °C for the applied flux density wave shapes at 530 kHz gives for 3F3 1030 mW/cm^3 and for 3F4 1580 mW/cm^3. Clearly 3F3 is the best option
The temperature rise induced in the E-PLT14 is given by:

(calculated loss density 3F3/allowed loss density) . ½ΔT
= (1030/1225) . 25°C = 21 °C.

For the E-E14 combination this would be 23.5 °C.
For the primary side 7 or 14 turns are required, depending on the input voltage. For a conventional forward transformer the same number of turns is necessary for the demagnetizing (recovery) winding. To make it possible to use 7 or 14 primary turns and the same number of turns for the demagnetizing winding, 4 layers with each 7 turns are chosen. When 7 primary and demagnetizing turns are needed, the turns on 2 layers are connected in parallel. This will give the additional effect that the current density in the winding tracks will be halved.
If 14 turns are necessary for the primary and demagnetizing windings, the turns in two layers are connected in series so that the effective number of turns is 14.

The available winding width for a PCB for the E 14 core is 3.65 mm. For an economic design with 300 µm spacing the track width for 7 turns per layer is 178 µm.

The copper layer thickness should be 70 µm because for the 24 V input the effective primary current is about 1.09 A. This gives (see fig. 2) in an effective track width of 356 µm (double because of parallel connection for 7 winding turns) a temperature rise of 15 °C The 48 V input will result in an effective current of about 0.54 A. This will give in a track width of 178 µm (14 winding turns connected in series) a winding loss contribution to the temperature rise of approx. 14 °C.

Core	Vin	Vout	N_1	N_2	Lprim (µH)	Io(RMS) (mA)	Imag (mA)	Ip(RMS) (mA)
E-PLT14	48 V	5 V	14	3.2	690	2441	60	543
	48 V	3.3 V	14	2.1	690	3699	60	548
	24 V	5 V	7	3.2	172	2441	121	1087
	24 V	3.3 V	7	2.1	172	3699	121	1097
E-E14	48 V	5 V	14	3.2	855	2441	48	539
	48 V	3.3 V	14	2.1	855	3699	48	544
	24 V	5 V	7	3.2	172	2441	97	1079
	24 V	3.3 V	7	2.1	172	3699	97	1089

Table 4: Calculation of several forward transformers

The track width of 178 µm with spacings of 300 µm for 70 µm Cu thickness deviates a little from the rule of thumb (spacing and track width > 200 µm). This might give rise to somewhat higher production costs for the multilayer PCBs.
The secondary winding requires 3 or 2 turns. When these turns are put in only one layer each, track widths of 810 and 1370 µm respectively result. The secondary RMS currents of 2.44 and 3.70 A induce a temperature rise of about 25 °C in the windings which is, added to the temperature rise in the primary windings, too high.
In this case the best solution is to use 2 layers for both windings. When these layers with 3 turns each are connected in parallel the current density is halved. From fig 2. it can be deduced that the winding loss contribution to the temperature rise in this situation will be about 6°C.
The total temperature rise of the PCB will be approximately 21 °C plus the addition caused by the AC losses. Since the frequency is 500 kHz this will be about 10 °C more, so the temperature of the PCB will increase by 31 °C.

The complete structure of the layer design is shown in table 5. At least 1 extra layer, denoted in the table as track layer, is necessary to make some interconnections.
However this would mean a total number of 9 layers, which from the manufacturing point of view is the same as 10 (the next even number).For this reason both the top and bottom layers of the PCB are used as track layers, also because it has the additional advantage that current densities in the tracks are cut in half. The tracks in these layers are connected to the tracks in the inner layer via copper plated holes and are "transporting" the in and outputs of the primary and secondary to two different sides of the PCB. Depending of how the connections of the in and outputs on the secondary and primary side are made, 4 different transformation ratios can be obtained.

The total nominal thickness of the PCB will be about 2.6 mm which is too high for the available winding window of 1.8 mm of an E-PLT14 core set combination. An E-E14 combination is suitable, however the minimum winding window of this core set is 3.6 mm which is much more than what is really required. A customized core shape with a reduced height is a better solution.
The real temperature on this PCB was measured with thermocouples under various conditions. The 24-5 volt transformation which gives rise to the highest current densities was used for the check.
First the calculated primary and secondary currents were supplied to the PCB separately as DC. The primary DC current of 1079 mA gave a temperature rise of 12.5°C, the secondary current of 2441 mA a rise of 7.5 °C. As could be expected when the two DC currents were supplied simultaneously to the PCB the temperature increase was 20°C.

The procedure has been repeated for the same RMS currents, but this time as AC at several frequencies. At 500 kHz the total temperature rise on the PCB was 32°C.
The strongest increase in temperature rise caused by the AC currents (7°C) is found in the secondary windings. This is logical because the influence of the skin effect will be larger in the wider secondary windings than in the narrow primary tracks.

Finally the temperatures have been measured when the PCB was combined with the standard E-E14 core set and subjected to the operational conditions as forward transformer.
On the PCB a temperature rise of 49 °C occurred while the hot spot of the core was on the top side with a temperature rise of 53 °C.
The centre leg and outer leg showed a temperature rise of 49 °C and 51 °C respectively.

As predicted by the calculations the design is somewhat critical for the E-E core set because the temperature rise of the hot spot is 53 °C i.s.o. 50 °C. However by using a flatter (customized) E-E core set the temperatures will drop within the limits of the specification.

Layers	Turns	70 µm
solder mask		50 µm
tracks layer		70 µm
insulation		200 µm
primary demag.	7	70 µm
insulation		200 µm
primary	7	70 µm
insulation		200 µm
secondary	3	70 µm
insulation		200 µm
secondary	2	70 µm
insulation		200 µm
secondary	2	70 µm
insulation		200 µm
secondary	3	70 µm
insulation		200 µm
primary	7	70 µm
insulation		200 µm
primary demag.	7	70 µm
insulation		200 µm
tracks layer		70 µm
solder mask		50 µm
TOTAL		**2600 µm**

Table 3. Example of a 10 layers design

References

1. Mulder S.A., 1990
Application note on the design of low profile high frequency transformers, Ferroxcube Components.

2. Mulder S.A.,1994
Loss formulas for power ferrites and their use in transformer design,Philips Components.

3. Durbaum Th, Albach M, 1995
Core losses in transformers with an arbitrary shape of the magnetizing current.1995 EPE Sevilla.

4. Brockmeyer A., 1995
Experimental Evaluation of the influence of DC premagnetization on the properties of power electronic ferrites, Aachen University of Technology

5. Ferroxcube Components technical note, 1996
25 Watt DC/DC converter using integrated Planar Magnetics.(9398 236 26011)

Appendix 1: Formulas used for the calculations of the design

List of symbols used

A_e	=	effect. cross-sectional area	N_{IC}	=	windings for IC voltage
B_{peak}	=	peak flux density	P_{max}	=	output power
f	=	Switching frequency	U_{imin}	=	minimum input voltage
$I_{p(RMS)}$	=	primary rms current	U_0	=	output voltage
$I_{0(RMS)}$	=	secondary output current	U_{IC}	=	IC voltage
I_{mag}	=	magnetizing current (forward)	δ	=	duty cycle signal (forward)
L_{prim}	=	primary self inductance	δ_{prim}	=	duty cycle primary signal
l_e	=	effect. path length	δ_{sec}	=	duty cycle secondary signal
G	=	airgap length	μ_a	=	amplitude permeability
N_1	=	primary winding turns	μ_e	=	effective permeability
N_2	=	secondary winding turns	μ_0	=	permeability of free space

formulas for flyback transformers

$$N_1 = \frac{U_{imin} \cdot \delta_{prim}}{2 \cdot f \cdot B_{peak} \cdot A_e}$$

$$N_2 = \frac{N_1 \cdot U_o \cdot \delta_{sec}}{U_{imin} \cdot \delta_{prim}}$$

$$N_{IC} = \frac{U_{IC} \cdot N_1}{U_{imin}}$$

$$L_{prim} = \frac{(U_{imin} \cdot \delta_{prim})^2}{2 \cdot P_{max} \cdot f}$$

$$G = \frac{\mu_0 \cdot N_1^2 \cdot A_e}{L_{prim}}$$

$$I_{o(RMS)} = \frac{P_{max}}{U_o} \cdot \sqrt{\frac{4}{3 \cdot \delta_{sec}}}$$

I_{mag} = not applicable

$$I_{p(RMS)} = \frac{U_{imin} \cdot \delta_{prim}}{f \cdot L_{prim}} \cdot \sqrt{\frac{\delta_{prim}}{3}}$$

formulas for forward transformers

$$N_1 = \frac{U_{imin} \cdot \delta}{2 \cdot f \cdot B_{peak} \cdot A_e}$$

$$N_2 = \frac{N_1 \cdot U_o}{U_{imin} \cdot \delta}$$

N_{IC} = not applicable

$$L_{prim} = \frac{\mu_0 \cdot \mu_a \cdot N_1^2 \cdot A_e}{l_e}$$

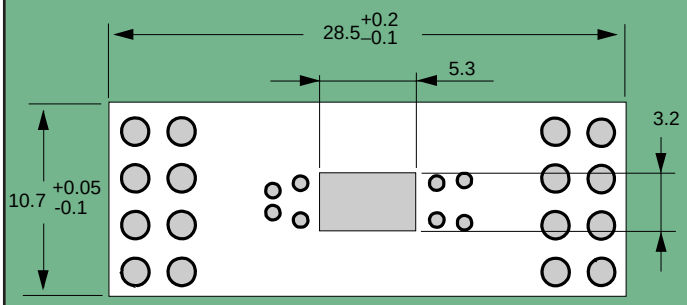
G = not applicable

$$I_{o(RMS)} = \frac{P_{max}}{U_o} \cdot \sqrt{\delta}$$

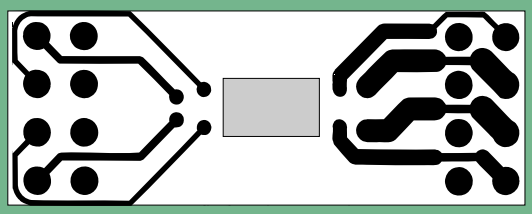
$$I_{mag} = \frac{U_{imin} \cdot \delta}{f \cdot L_{prim}}$$

$$I_{p(RMS)} = \frac{I_{o(RMS)}}{r} + \frac{I_{mag}}{2} \cdot \sqrt{\delta}$$

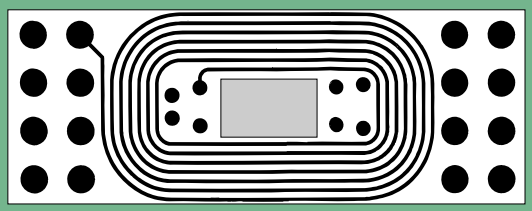
Appendix 2: Layer design for the planar E 14 forward transformer



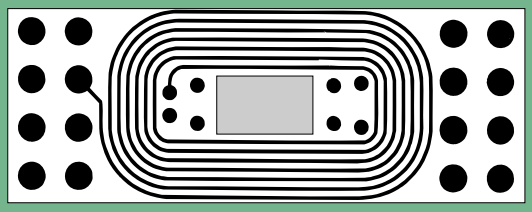
hole pattern



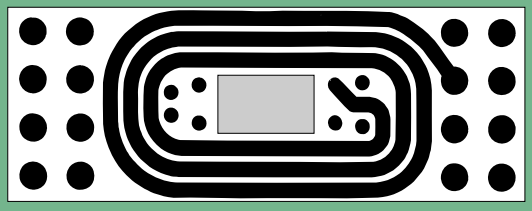
layer 1 (top)



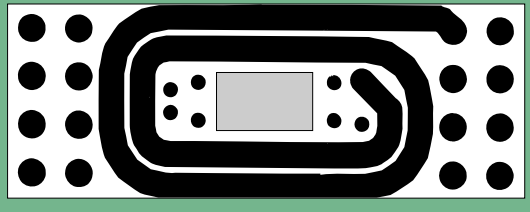
layer 2



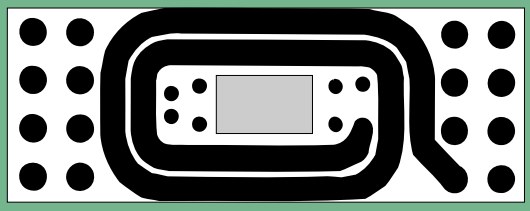
layer 3



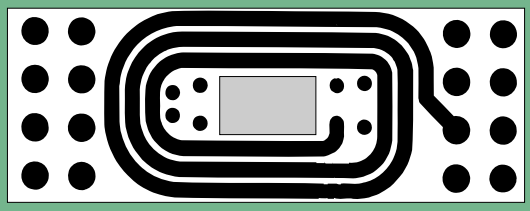
layer 4



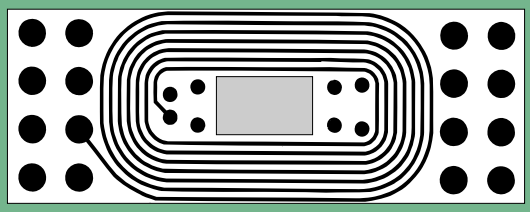
layer 5



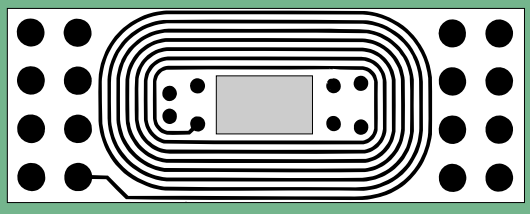
layer 6



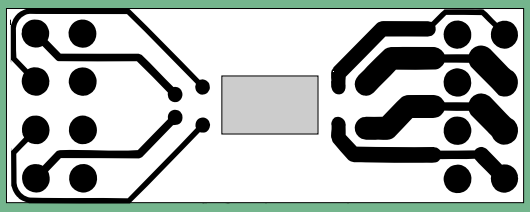
layer 7



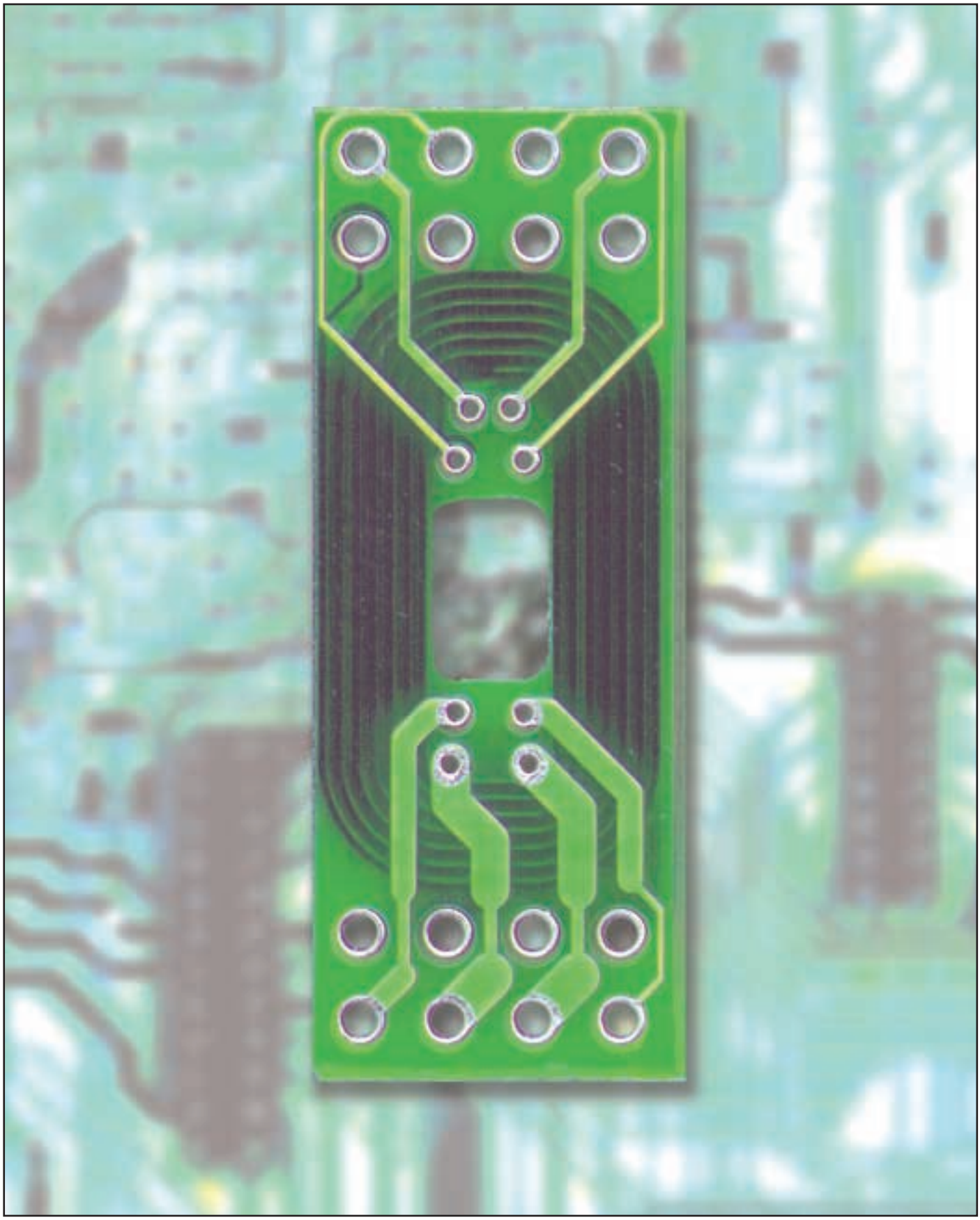
layer 8



layer 9



layer 10 (bottom)



Top view of the example multilayer PCB